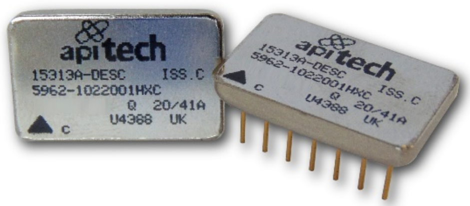
Model # 15313

Nuclear Event Detector (NED) Data Sheet



A Nuclear Event Detector (NED) is an essential element of any nuclear hardened electronic system hardware. It provides sensing and response signals to ionizing radiation pulses emitted during nuclear events.

Under such conditions, the NED, with a customer programmed threshold (external resistor) will provide two outputs:

- A timed output (set by an external capacitor)
- A latched output with electrical reset

The module is supplied in a 14 pin military standard hermetic package that is fully tested and compliant with military requirements. It is capable of detecting short duration pulses and has a number of features including a test input to verify functional health.

Features

- Detection of ionising radiation above a pre-set level
- Ability to set a trigger threshold by a single external resistor (RTH)
- Provision of a fast pulsed detected output ($\overline{\mathrm{NED}}$)
- Ability to set the $\overline{\mathrm{NED}}$ output pulse duration by a single external capacitor (CA to CB)
- Provision of a fast latched flag output ($\overline{\mathrm{NEF}}$)
- Provision of complementary flag reset inputs (FR and $\overline{\mathrm{FR}}$)
- Provision of a separate supply for the main electronics (VH)
- Provision of a separate bias supply for the detection diode (VB)
- Provision of a separate load supply for the output drive transistors (VL)
- Operation within specification across the military temperature range (-55°C to +125°C)

Maximum Ratings

Parameter	Limit
Voltage at pins 6, 11, 12 and 14 w.r.t. pin 7	**7.0 V**
Voltage at pin 1 w.r.t. pin 7	**20 V**
Voltage at pin 8 w.r.t. pin 7	**5.5 V**
Storage temperature range	**-65°C < Ta < +150°C**
Ionising radiation dose rate (operate through and survive)	**>1E8 Gy(Si)/s**
Ionising total dose	**>100 Gy(Si)**
Neutron fluence	**>1E13 n/cm^2**

Table 1 Pin Description

Pin	Name	Function	Description
1	V_L	SUPPLY	Output pull-up supply
2	$\overline{\mathrm{NED}}$	OUTPUT	Nuclear Event Detector pulsed output
3	NC3	n/c	
4	C_B	INPUT	Timing capacitor (negative)
5	C_A	OUTPUT	Timing capacitor (positive)
6	TEST	INPUT	Built in Test input
7	GND	GROUND	Device supply ground and case connection
8	V_B	SUPPLY	Device detector bias supply
9	R_{TH}	INPUT	Threshold set input
10	NC10	n/c	
11	NFR	INPUT	Flag reset inverse input
12	FR	INPUT	Flag reset input
13	NEF	OUTPUT	Nuclear Event Flag output
14	V_H	SUPPLY	Device Supply

TRIGGER THRESHOLD SETTING

The NED has provision for setting a nominal trigger threshold between 1E3 & 1E6 Gy(Si)/s using a single external resistor. The threshold is a product of the resistor value (Fig. 2) and radiation pulse width (Fig. 3). The following equation can be used :-

$$DR = \frac{2.18E7}{Rth/(1 - e^{\left(-\frac{125tp}{Rth}\right)})}$$

DR= radiation pulse amplitude in Gy/s
Rth = resistor value
tp = rectangular radiation pulse width in ns
1 Gy/s = 100 rad/s

$\overline{NED}$ PULSE DURATION SETTING

The duration of the $\overline{\mathrm{NED}}$ pulse width is set by an external capacitor connected between the Ca and Cb pins. The nominal calculation is 20us/nF.
The pulse width should be set long enough to protect the system from the initial event until radiation has fallen to safe levels at which the system can operate.

TABLE 2. Electrical performance characteristics

Parameter	Symbol	Conditions -55°C ≤ T_A ≤ +125°C unless otherwise specified	Limits			Unit
			Min	Typ	Max	
Standby Supply Current	I_H	Supply voltage V_H = 5.5V, TEST Input = 0.00V to 0.05V, NFR Input = 4.5V to 5.5V, FR Input = 0.00V to 0.05V, $\overline{NED}$ and $\overline{NEF}$ outputs high (>4.5V)			2.0	mA
Flag Set Supply Current	I_H	V_H = 5.5V, $\overline{NED}$ output >4.5V, $\overline{NEF}$ output <0.5V			6.0	mA
Operational Supply Current	I_H	V_H = 5.5V, $\overline{NED}$ and $\overline{NEF}$ outputs <0.5V			15.0	mA
Output Leakage Current	I_L	VL = 20.0V, $\overline{NED}$ and $\overline{NEF}$ outputs >4.5V			100	uA
Detector Leakage Current	I_B	Detector bias voltage V_B = 5.5V, $\overline{NED}$ output >4.5V, $\overline{NEF}$ output <0.5V			5.0	uA
Detector Forward Voltage	V_F	Forward current, I_{TH} = 10mA	0.25		1.0	V
FR Input Current	I_{FR}	Flag reset voltage V_{FR} = 0.7V, R_{TH} not connected (note 6)		0.5	1.0	mA
	I_{FR}	Flag reset voltage V_{FR} = 3.0V, R_{TH} not connected (note 6)		2.3	3.0	mA
FR Switching Voltage	V_{FRSW}	R_{TH} not connected (note 6)	0.7	2.1	3.0	V
$\overline{FR}$ Input Current	I_{NFR}	$\overline{FR}$ voltage V_{NFR} = 0.7V, R_{TH} not connected (note 6)		-0.5	-3.0	mA
	I_{NFR}	$\overline{FR}$ voltage V_{NFR} = 4.0V, R_{TH} not connected (note 6)		-0.1	-1.0	mA
$\overline{FR}$ Switching Voltage	V_{NFRSW}	R_{TH} not connected (note 6)	0.7	1.6	2.0	V
TEST Input Current	I_{TEST}	TEST voltage V_{TEST} = 0.7V		0.5	1.0	mA
	I_{TEST}	TEST voltage V_{TEST} = 4.0V		3.3	4.0	mA
TEST Switching Voltage	V_{TESTSW}		0.7	2.1	3.0	V
$\overline{NED}$ Output Voltage	V_{DOH}	V_L = 20V, $\overline{NED}$ output current I_O = -100µA	18.5			V
	V_{DOL}	$\overline{NED}$ output current I_{OL} = 10mA			0.6	V
	V_{DOL}	$\overline{NED}$ output current I_{OL} = 20mA			0.7	V
$\overline{NEF}$ Output Voltage	V_{FOH}	V_L = 20V, $\overline{NEF}$ output current I_O = -100µA	18.5			V
	V_{FOL}	$\overline{NEF}$ output current I_{OL} = 10mA			0.6	V
	V_{FOL}	$\overline{NEF}$ output current I_{OL} = 20mA			0.7	V
TEST Input pulse width	t_{TEST}	V_{TEST} = 0V to 4.0V	250			ns
TEST to $\overline{NED}$ or $\overline{NEF}$ delay	t_o	V_{TEST} = 0V to 4.0V duration 10µs		5	10	us
FR Input pulse width	t_{FR}	V_{FR} = 0V to 4.0V	250			ns
FR Input to $\overline{NEF}$ Delay	t_r	V_{FR} = 0V to 4.0V duration 1µs		0.2	1.0	us
$\overline{FR}$ Input pulse width	t_{NFR}	V_{NFR} = 5.0V to 0.7V	500			ns
$\overline{FR}$ Input to $\overline{NEF}$ delay	t_s	V_{NFR} = 5.0V to 0.7V duration 1µs		0.25	1.0	µs
$\overline{NED}$ Output Delay	t_t	V_{RTH} = 0V to 5.0V duration 100ns, pull-up resistor =220Ω		25	50	ns
$\overline{NEF}$ Output Delay	t_u	V_{RTH} = 0V to 5.0V duration 100ns, pull-up resistor =220Ω		50	200	ns
$\overline{NED}$ output pulse width	t_{NED}	Supply voltage V_H = 4.5V to 5.5V, pulse duration timed from negative edge of TEST input	10	20	30	us/nF
$\overline{NED}$ Output Pulse Width	t_{NED}	Supply voltage V_H = 4.95V to 5.05V	13	20	27	µs/nF

Footnotes for Table 2:

1. All voltage measurements are made with respect to pin 7 (GND) unless otherwise stated.
2. The definition of low and high voltage levels are: V_{OL} < 0.5V, V_{OH} > 4.5V unless otherwise stated.
3. V_L and V_H = 4.5V to 5.5V unless otherwise stated.
4. V_B, $\overline{NED}$ and $\overline{NEF}$ are not connected unless otherwise stated.
5. C_T = 47nF +/-10% and connected to pins 4 and 5 unless otherwise stated.
6. R_{TH} = 180Ω +/-2% connected between pin 9 (RTH) and pin 7 (GND) unless otherwise stated.
7. In standby mode (no nuclear event detected) both $\overline{NED}$ and $\overline{NEF}$ outputs and NFR input will be in the 'high' state and TEST and FR input will be in the 'low' state.

TABLE 3. Truth Table

				Time - ▯	t = 0s	t = 0s	After t_o	After t_q	After t_p	After t_p	After t_r
STATUS	TEST	$\overline{FR}$		FR	$\overline{NED}$	$\overline{NEF}$	$\overline{NED}$	$\overline{NEF}$	$\overline{NED}$	$\overline{NEF}$	$\overline{NEF}$
Standby	L	H		L	H	H	H	H	H	H	H
Nuclear event detection (or simulation)	H	H		L	H	H	L	L	H	L	H
After nuclear event detection (or simulation)	L	H		L	L	L	L	L	H	L	H
Reset by FR input	L	H		H	H	L	N/A	N/A	N/A	N/A	H
Reset by NFR input	L	L		L	H	L	N/A	N/A	N/A	N/A	H

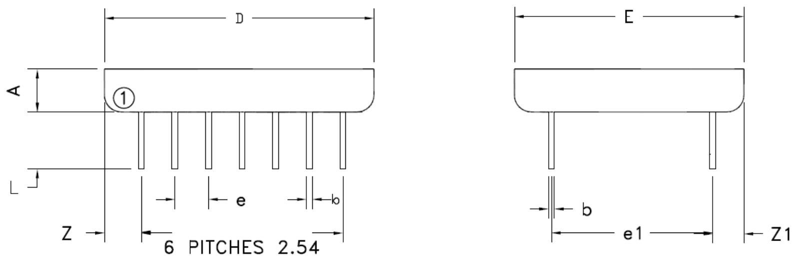
Footnotes for Table 2:

1. Time t_o is the delay between the TEST input voltage rising to 90% of its peak voltage and the NED output falling to 10% of its peak voltage.
2. Time t_p is the width of the pulse from the NED output measured between the falling and rising edges at 50% of the amplitude.
3. Time t_q is the delay between the TEST input voltage rising to 90% of its peak voltage and the NEF output falling to 10% of its peak voltage.
4. Time t_r is the delay between the FR input voltage rising to 90% of its peak voltage and the NEF output rising to 90% of its peak voltage.
5. Time t_s is the delay between the NFR input voltage falling to 10% of its peak voltage and the NEF output rising to 90% of its peak voltage.
6. Outputs inactive during power up provided V_H rises at < 5000 V/s (5 V/ms)

PART ORDERING INFORMATION

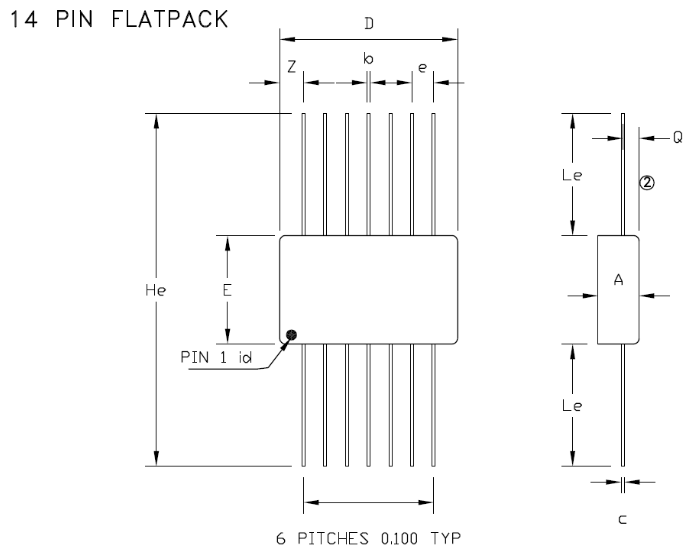
Part Number	**Feature**	**Option**
5962-1022001HXC	14 pin DIL as per DLA SMD 5962-10220	gold plate finish leads
5962-1022001HXA	14 pin DIL as per DLA SMD 5962-10220	hot solder dip finish leads
15313	14 pin DIL case outline	gold plate finish leads
15313A	14 pin DIL case outline	hot solder dip finish leads
14907	14 pin flatpack case outline	gold plate finish leads
14907A	14 pin flatpack case outline	hot solder dip finish leads

Figure 2. DIL Case Outline



REF	DIMENSIONS mm			DIMENSIONS in		
	MIN	NOM	MAX	MIN	NOM	MAX
D	20.06	20.19	20.32	0.790	0.795	0.800
E	12.44	12.57	12.70	0.490	0.495	0.500
A	–	3.56	3.69	–	0.140	0.145
L	4.95	5.08	5.21	0.195	0.200	0.205
b	–	0.46	–	–	0.018	–
e	–	2.54	–	–	0.100	–
e1	–	7.62	–	–	0.300	–
Z	–	2.46	–	–	0.097	–
Z1	–	2.46	–	–	0.097	–

Figure 3. FP Case Outline



REF.	MIN.	NOM.	MAX.
D	0.815	0.820	0.825
E	0.485	0.490	0.495
LE	0.450	–	–
e	–	0.100	–
Z	0.105	0.110	0.115
b	0.012	0.015	0.018
Q	–	0.075	–
He	1.385	–	–
c	0.008	0.010	0.012
A	–	0.145 TYP	–