50μsec, 12-bit Military A/D Converters

FEATURES

- 50μsec Maximum Conversion Time
- ±1/2LSB Linearity and No Missing Codes Guaranteed Over Temperature
- Small 24-Pin DIP
- ±1LSB Zero Error
- ±2LSB Absolute Accuracy
- Full Mil Operation −55°C to +125°C
- MIL-PRF-38534 Screening Optional

DESCRIPTION

MN5200 Series devices are 12-bit, successive approximation A/D converters in industry-standard, 24-pin, dual-in-line packages. Functional laser trimming of our own nichrome thin-film resistor networks results in adjustment-free devices that are extremely accurate and highly stable.

Zero error, for example, is guaranteed to be better than ±0.025% FSR (±1 LSB) at +25°C and better than ±0.05% FSR (±2 LSB) over the entire operating temperature range. All units are fully specified and 100% tested for linearity and accuracy at their operating temperature extremes as well as at room temperature.

These A/D converters are available in a number of input voltage ranges. For each range, the user has the option of specifying a model complete with internal reference or, for improved overall accuracy, a model which uses an external reference. In all cases, ±½LSB linearity and 12-bit "no missing codes" are guaranteed over the entire operating temperature range.

All models of the MN5200 Series may be procured for operation over the full −55°C to +125°C military temperature range ("H" models) or the 0°C to +70°C commercial temperature range. For military/aerospace or harsh-environment commercial/industrial applications "H/B CH" models are fully screened to MIL-PRF-38534, class H requirements.

The MN5200 Series (50μsec conversion time) and MN5210 Series (13μsec conversion time) are the industry's most widely accepted 12-bit A/D's for military/aerospace applications. These devices are presently designed into more than 50 military/aerospace programs. Their small size, low power consumption and adjustment-free operation make them excellent selections for compact, highly reliable systems. New applications will be found wherever size, speed, power and temperature considerations are paramount.

MN5200 SERIES 50μsec 12-Bit MILITARY A/D CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	0°C to +70°C -55°C to +125°C ("H" Models)
Storage Temperature	-65°C to +150°C
Positive Supply (Pin 15)	+18 Volts
Negative Supply (Pin 13)	-18 Volts
Logic Supply (Pin 2)	-0.5 to +7 Volts
Analog Input (Pin 14)	±25 Volts
Digital Inputs (Pins 1, 24)	-0.5 to +5.5 Volts
Digital Outputs	Logic Supply
Ref. Input (MN5203, 04, 05)	0 to -15 Volts

ORDERING INFORMATION

PART NUMBER — MN520X H/B CH

- Select Model Number (MN5200, MN5201 etc.)
- Standard part is specified for 0°C to +70°C operation.
- Add "H" for specified −55°C to +125°C operation.
- Add "/B" to "H" models for Environmental Stress Screening.
- Add "CH" to "/B" models for 100% screening according to MIL-PRF-38534.

SPECIFICATIONS (T_A = +25°C, Supply Voltages ±15V and ±5V, for Ext. Ref. Models V_{Ref} = −10.000V, unless otherwise specified).

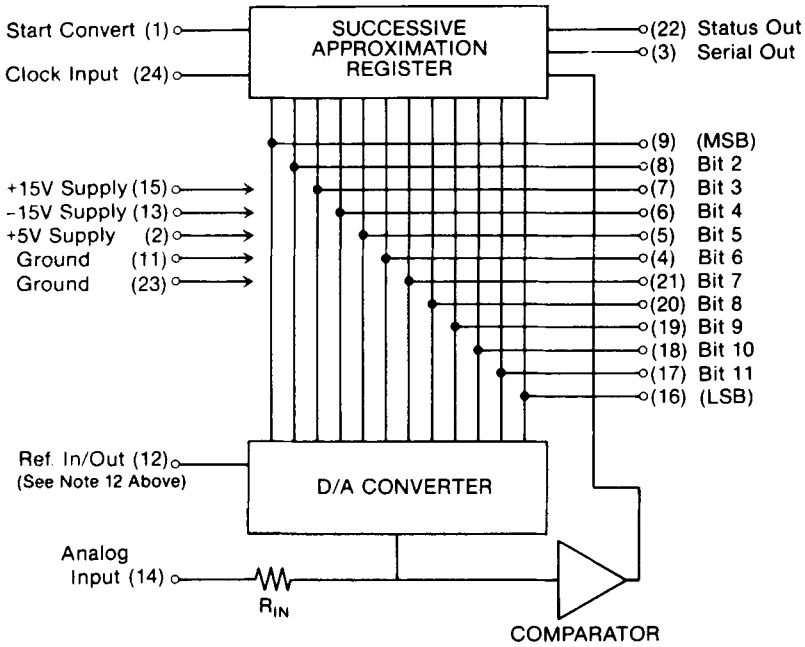
ANALOG INPUTS	MODEL NUMBER		MODEL NUMBER		
Input Range (Input Impedance) (Note 1): 0 to −10V (5KΩ) −5V to +5V (5KΩ) −10V to +10V (10KΩ) 0 to +10V (5KΩ)	(Internal Ref.) MN5200 MN5201 MN5202 MN5206		(External Ref.) MN5203 MN5204 MN5205		
TRANSFER CHARACTERISTICS	**TYP.**	**MAX.**	**TYP.**	**MAX.**	**UNITS**
Linearity Error (Notes 2, 3): +25°C 0°C to +70°C −55°C to +125°C ("H" Models)	±¼ ±¼	±½ ±½ ±½	±¼ ±¼	±½ ±½ ±½	LSB LSB LSB
Differential Linearity Error	±½		±½		LSB
No Missing Codes	Guaranteed Over Temperature				
Full Scale Absolute Accuracy Error (Notes 4, 5) +25°C 0°C to +70°C −55°C to +125°C ("H" Models)	± 0.25 ± 0.2	± 0.05 ± 0.4 ± 0.4	± 0.025 ± 0.05	± 0.05 ± 0.1 ± 0.1	%FSR %FSR %FSR
Zero Error (Notes 4, 5): +25°C 0°C to +70°C −55°C to +125°C ("H" Models)	± 0.01 ± 0.025	± 0.025 ± 0.05 ± 0.05	± 0.01 ± 0.025	± 0.025 ± 0.05 ± 0.05	%FSR %FSR %FSR
Gain Error (Note 5) Gain Drift	± 0.025 ± 10		± 0.025 ± 3		% ppm/°C
Conversion Time (Note 6)		50		50	μSec
POWER SUPPLIES					
Power Supply Range: ±15V Supplies +5V Supply		± 3 ± 5		± 3 ± 5	% %
Power Supply Rejection (Note 7): +15V Supply −15V Supply	± 0.005 ± 0.01	± 0.02 ± 0.05	± 0.005 ± 0.005	± 0.02 ± 0.02	%FSR/% Vs %FSR/% Vs
Current Drain: +15V Supply −15V Supply +5V Supply −10V Reference (MN5203, 04, 05)	23 −25 25	28 −35 42	23 −25 25 −1.5	28 −35 42 −2	mA mA mA mA

DIGITAL INPUTS (ALL UNITS)	MIN.	TYP.	MAX.	UNITS
Logic Levels: Logic "1" Logic "0"	2.0		 0.7	Volts Volts
Clock Input (Note 8): Pulse Width High Pulse Width Low Loading High (V_{in} = 2.4V) Loading Low (V_{in} = 0.3V) Frequency (Note 6)	125 175	 2 −0.25	 20 −0.4 240	nSec nSec μA mA KHz
Start Convert Input: Loading High (V_{in} = 2.4V) Loading Low (V_{in} = 0.3V) Setup Time Start Low to Clock (Note 9)	 25	4 −0.25	40 −0.4	μA mA nSec
DIGITAL OUTPUTS (ALL UNITS)				
Logic Coding (Note 10): Unipolar Ranges Bipolar Ranges	Complementary Straight Binary Complementary Offset Binary			
Logic Levels: Logic "1" Logic "0"	2.4	3.6 0.15	 0.3	Volts Volts
Output Drive Capability, All Outputs (Note 11): Logic "1" Logic "0"	8 2			TTL Loads TTL Loads
REFERENCE INPUT/OUTPUT (Note 12)				
Internal Reference: Voltage Accuracy Tempco of Drift Max. External Current (Without Buffering)		−6.3 ±2 ±5	 100	Volts % ppm/°C μA
External Reference: Voltage Loading		−10.000	 − 2	Volts mA

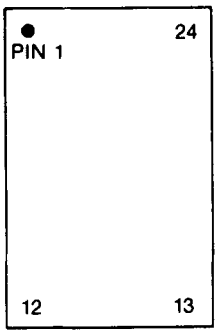
SPECIFICATION NOTES:

1. Consult factory for other available input voltage ranges.
2. Micro Networks tests and guarantees maximum linearity error at room temperature and at both the high and low extremes of the specified operating temperature range.
3. 1 LSB for a 12 bit converter corresponds to 0.024%FSR. See Note 4.
4. FSR stands for Full Scale Range and is equal to the peak to peak voltage of the selected input range. For the ±10V input range, FSR is 20 volts, and 1 LSB is equal to 4.88 mV. For the 0 to +10V, 0 to -10V, and ±5V ranges, FSR is 10 volts, and 1 LSB is equal to 2.44 mV.
5. See Absolute Accuracy section below for an explanation of how Micro Networks tests and specifies Full Scale Absolute Accuracy, Gain, and Zero Errors.
6. Conversion Time is defined as the width of the converter's STATUS (E.O.C.) pulse. See Timing Diagram. For the MN5200 Series, a 50 μSec conversion time corresponds to an external clock frequency of 240 kHz. Micro Networks guarantees Linearity and Absolute Accuracy at and below this clock frequency.
7. Micro Networks tests and guarantees Power Supply Rejection over the ±15V ±3% range.
8. The clock may be asymmetrical with minimum positive or negative pulse width. See Note 6.
9. In order to reset the converter, START CONVERT must be brought low at least 25 nSec prior to a low to high clock transition. See Timing Diagram.
10. CSB = Complementary Straight Binary
    COB = Complementary Offset Binary
    Serial and parallel output data have the same coding. Serial data is in Non-Return to Zero (NRZ) format. See Output Coding and Timing Diagram.
11. One TTL load is defined as sinking 40 μA with a logic "1" applied and sourcing 1.6 mA with a logic "0" applied.
12. MN5200, MN5201, MN5202, and MN5206 have an internal -6.3V reference. MN5203, MN5204, and MN5205 require an external -10.000V reference.

BLOCK DIAGRAM



PIN DESIGNATIONS

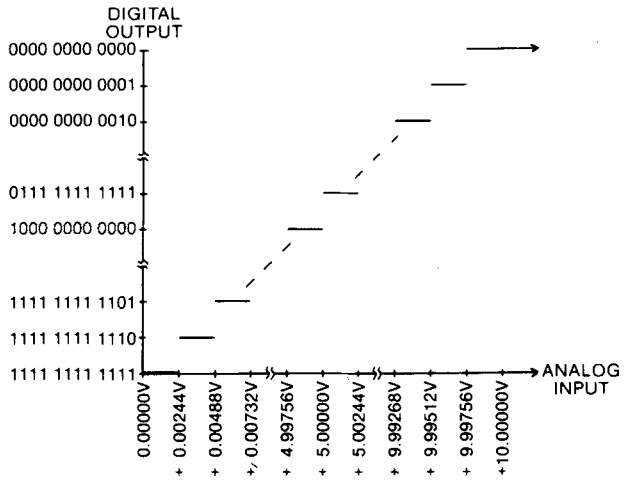


Pin 1	Start Convert	Pin 24	Clock Input
Pin 2	+5V Supply	Pin 23	Ground
Pin 3	Serial Output	Pin 22	Status (E.O.C.)
Pin 4	Bit 6	Pin 21	Bit 7
Pin 5	Bit 5	Pin 20	Bit 8
Pin 6	Bit 4	Pin 19	Bit 9
Pin 7	Bit 3	Pin 18	Bit 10
Pin 8	Bit 2	Pin 17	Bit 11
Pin 9	Bit 1 (MSB)	Pin 16	Bit 12 (LSB)
Pin 10	N/C	Pin 15	+15V Supply
Pin 11	Ground	Pin 14	Analog Input
Pin 12	Ref. Out (-6.3V) Ref. In (-10.0V)	Pin 13	-15V Supply

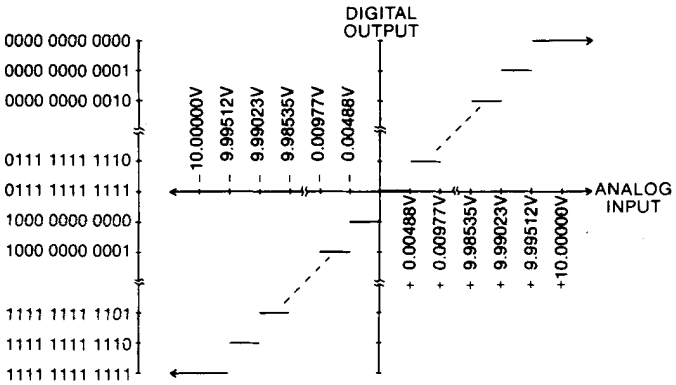
ABSOLUTE ACCURACY ERROR

A given digital output code is valid for a band of analog input voltages that is ideally 1 LSB wide. This is demonstrated in the next column and on the following page where portions of the theoretical analog input/digital output transfer functions of the MN5206 (0 to +10V input range) and the MN5202 (±10V input range) are sketched.

Notice that, for the MN5206, any analog input between +0.00244 volts (1 LSB = 2.44 mV) and +0.00488 volts will give a digital output of 1111 1111 1110. If we assign this code to the nominal midrange of the analog input band for which it is valid, we can say that the 1111 1111 1110 digital code corresponds to analog inputs of +3.66 mV ±1.22 mV which can be written as +3.66 mV ±1/2 LSB. The ±1/2 LSB is a quantization uncertainty unavoidable in A/D conversion. It is referred to as Inherent Quantization Error and its magnitude can be reduced only by going to higher resolution converters.



MN5206 TRANSFER FUNCTION



MN5202 TRANSFER FUNCTION

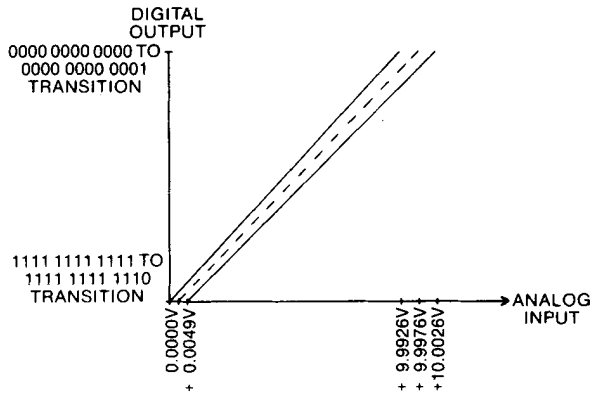
It is difficult and time consuming to measure the center of a quantization level (the +0.00366 volts in this example). The only points along an A/D converter's analog input/digital output transfer function that can quickly and accurately be detected and measured are the transition voltages, the voltages at which the digital outputs change from one code to the next. The *Absolute Accuracy Error* of a voltage input A/D converter is the difference between the actual, *unadjusted,* analog input voltage at which a *given* digital transition occurs and the analog input voltage at which that transition is ideally supposed to occur. This difference is usually expressed in LSB's or %FSR (see Note 4 above). Absolute Accuracy Error includes gain, offset, linearity, and noise errors, and when specified over temperature, encompasses the individual drifts of these errors.

For the MN5200 Series A/D converters, Micro Networks tests Absolute Accuracy Error at both endpoints of unipolar input ranges and at both endpoints and the midpoint of bipolar input ranges. These tests are performed at room temperature and at both the high and low extremes of the specified operating temperature range. The specifications appear in the table as the Full Scale Absolute Accuracy and Zero Errors.

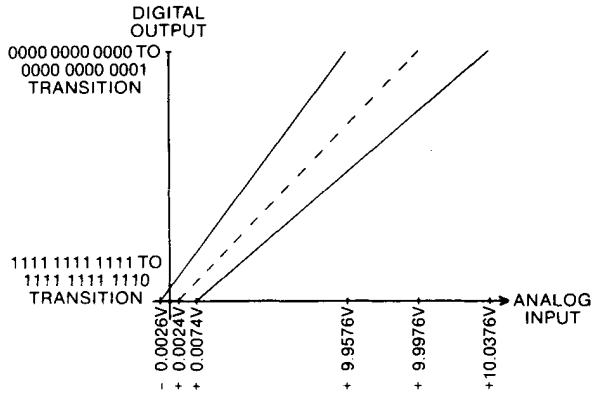
EXAMPLE MN5206: Return to the ideal analog input/digital output transfer function of the MN5206 sketched on page 3. Notice that the digital output data changes from 1111 1111 1111 to 1111 1111 1110 when the input voltage increases from 0V to +2.44 mV. It changes from 1111 1111 1110 back to 1111 1111 1111 as the input voltage is decreased from some more positive voltage to +2.44 mV. This voltage, +2.44 mV is the zero transition voltage. It is the voltage at which the LSB changes from a "1" to a "0" or vice versa while all other bits remain "1". The positive full scale LSB transition voltage, the voltage at which the LSB changes while the other bits remain "0", is ideally +9.9976V.

For the MN5206H (0 to +10V input range, -55°C to +125°C operation), Micro Networks tests linearity and the accuracy of the two transition voltages just discussed at -55°C, +25°C, and +125°C. We guarantee that the transfer function will be ±1/2 LSB linear at all temperatures and that the zero transition will be within ±0.025%FSR (±2.5 mV) of its ideal value (+2.44 mV) at +25°C and within ±0.05%FSR (±5 mV) of its ideal value at -55°C and at +125°C. This is our Zero Error specification. We guarantee that the positive full scale LSB transition voltage will be within ±0.05%FSR (±5 mV) of its ideal value (+9.9976V) at +25°C and within ±0.4%FSR (±40 mV) of its ideal value at -55°C and +125°C. This is our Full Scale Absolute Acuracy Error specification.

These Absolute Accuracy Error specifications are summarized in the two plots below. The ideal transfer function is now sketched as a broken line. We guarantee, for the MN5206H, that the actual transfer function will be ±1/2 LSB linear and that all the transition voltages will fall within the boundaries indicated by the solid lines at +25°C and at -55°C and +125°C.



MN5206 ABSOLUTE ACCURACY +25°C



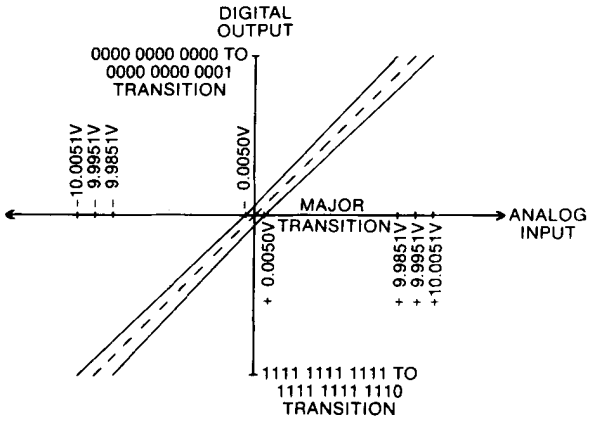
MN5206H ABSOLUTE ACCURACY -55°C AND +125°C

EXAMPLE MN5202: Return to the ideal analog input/digital output transfer function of the MN5202 sketched below. Notice that the digital output data changes from 1111 1111 1111 to 1111 1111 1110 when the input voltage increases from -10.000V to -9.9951V. It changes from 1111 1111 1110 back to 1111 1111 1111 as the input voltage is decreased from some more positive voltage to -9.9951V. This voltage, -9.9951V, is the negative full scale LSB transition voltage. It is the voltage at which the LSB changes from a "1" to a "0" or vice versa while all other bits remain "1". The 1000 0000 0000 to 0111 1111 1111 transition (called the "major transition" because all the bits change) ideally occurs at the zero volt analog input. The positive full scale LSB transition voltage, the voltage at which the LSB changes while the other bits remain "0", is ideally +9.9951V.

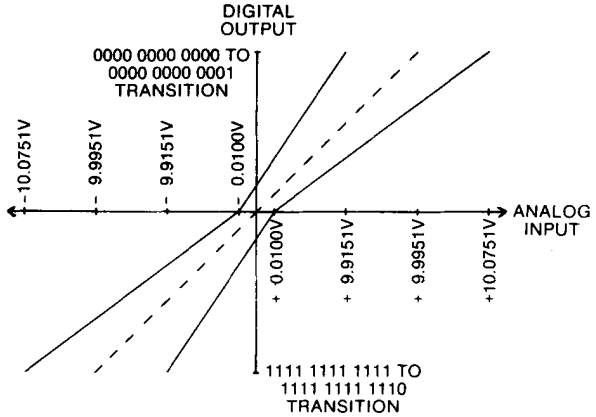
For the MN5202H (±10V input range, -55°C to +125°C operation), Micro Networks tests linearity and the accuracy of the three transition voltages just discussed at -55°C, +25°C, and +125°C. We guarantee that the transfer function will be ±1/2 LSB linear at all temperatures and that the positive and negative full scale LSB transition voltages will be within ±0.05%FSR (±10 mV) of their ideal values (+9.9951V and -9.9951V) at +25°C and within ±0.4%FSR (±80 mV) of their ideal values at -55°C and +125°C. This is our Full Scale

Absolute Accuracy Error specification. We also guarantee that the major transition voltage will be within ±0.025%FSR (±5 mV) of its ideal value (zero volts) at +25°C and within ±0.05%FSR (±10 mV) of its ideal value over the entire -55°C to +125°C operating temperature range. This is our Zero Error specification.

These Absolute Accuracy Error specifications are summarized in the two plots below. The ideal transfer function is now sketched as a broken line. We guarantee, for the MN5202H, that the actual transfer function will be ±1/2 LSB linear and that all the transition voltages will fall within the boundaries indicated by the solid lines at +25°C and at -55°C and +125°C.



MN5202 ABSOLUTE ACCURACY +25°C

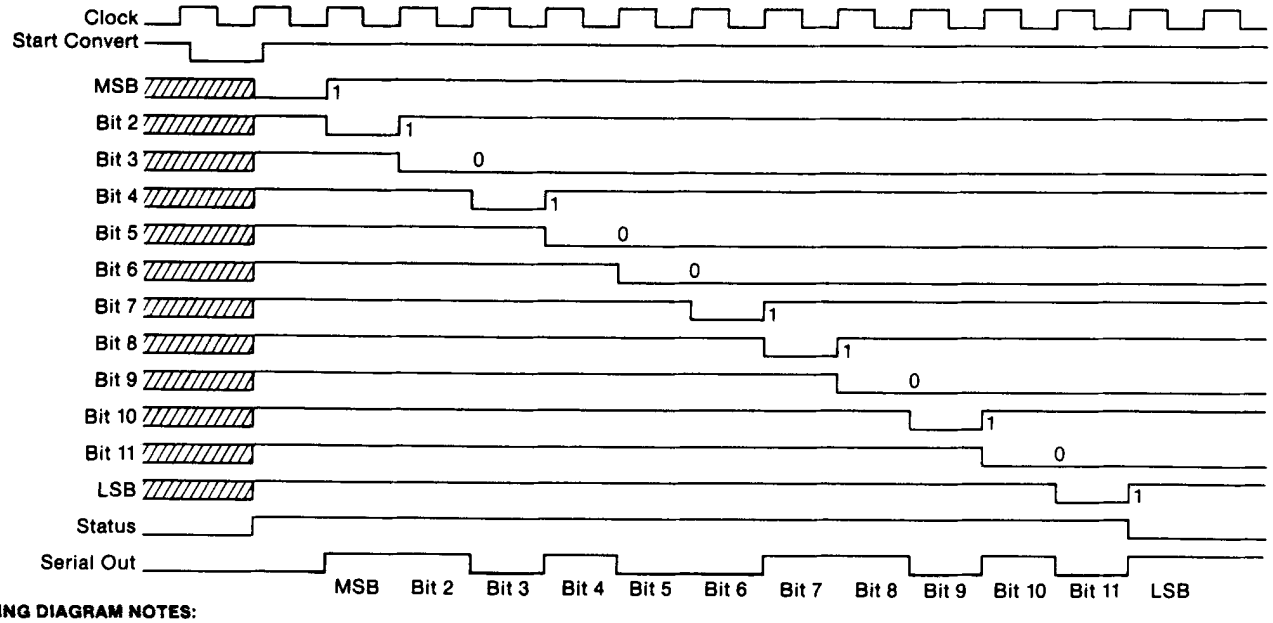


MN5202H ABSOLUTE ACCURACY -55°C AND +125°C

Because Micro Networks tests and guarantees ±1/2 LSB linearity at all temperatures, the Absolute Accuracy of any transition voltage can be interpolated from the Full Scale Absolute Accuracy and Zero Error specifications. Example: at +25°C, the 1000 0000 0000 to 0111 1111 1111 transition of the MN5206 will occur within ±0.0375%FSR (±3.75 mV) of its ideal value (+5.000V). For temperatures intermediate to +25°C and -55°C or +125°C, maximum Full Scale Absolute Accuracy and Zero Errors can also be interpolated. At +75°C, for example, Full Scale Absolute Accuracy Error will be ±0.225%FSR.

We have not specified Unipolar and Bipolar Offset Errors for the MN5200 Series. We feel that Offset is a confusing

TIMING DIAGRAM



TIMING DIAGRAM NOTES:

1. Operation shown is for the digital word 1101 0011 0101 which corresponds to 1.7432V on the 0 to +10V input range (MN5206). See Output Coding.
2. Conversion time is defined as the width of the STATUS (E.O.C.) pulse.
3. The converter is reset (MSB = "0", all other bits = "1", STATUS = "1") by holding the START CONVERT low during a low to high clock transition. The START CONVERT must be low for a minimum of 25 nSec prior to the clock transition. Holding the START low will hold the converter in the reset state. Actual conversion will begin on the next rising clock edge after the START has returned high.
4. The delay between the resetting clock edge and STATUS actually rising to a "1" is 120 nSec maximum.
5. The START CONVERT may be brought low at any time during a conversion to reset and begin converting again.
6. Both serial and parallel data bits become valid on the same rising clock edges. Serial data is valid on subsequent falling clock edges, and these edges can be used to clock serial data into receiving registers.
7. Output data will be valid 30 nSec (maximum) after the STATUS (E.O.C.) output has returned low. Parallel output data will remain valid and the STATUS output low until another conversion is initiated.
8. For continuous conversion, connect the STATUS output (Pin 22) to the START CONVERT input (Pin 1). See section on Continuous Conversion.
9. When the converter is initially "powered up", it may come on at any point in the conversion cycle.

specification and choose not to use it. Offset Errors for the MN5200 Series will always be equivalent to either our Full Scale Absolute Accuracy or Zero Errors and we prefer these specifications because of their simplicity. Be sure you clearly understand each manufacturer's converter specification definitions before you compare converters solely on a data sheet basis.

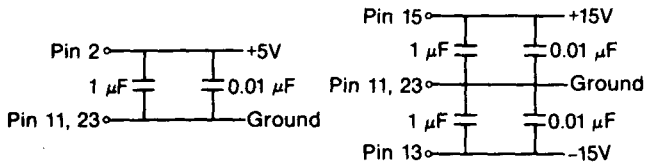
GAIN ERROR—Gain Error is the difference between the ideal and the measured values of a converter's Full Scale Range (minus 2 LSB); it is a measure of the slope of the converter's transfer function. Gain Error is not a type of Absolute Accuracy Error, but it can be calculated using two Absolute Accuracy Error measurements. It is equivalent to the Absolute Accuracy Error measured for the 0000 0000 0000 to 0000 0000 0001 transition minus that measured for the 1111 1111 1111 to 1111 1111 1110 transition.

See the Converter Tutorial Section of the Micro Networks' Applications Manual and Product Guide for a complete discussion of converter specifications.

APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracies from the MN5200 Series converters. The units' two GROUND pins (Pins 11 and 23) are not connected internally. They should be tied together as close to the package as possible and connected to system analog ground, preferably through a large ground plane underneath the package. If the grounds cannot be tied together and must be run separately, a non-polarized 0.01μF bypass capacitor should be connected between Pins 11 and 23 as close to the unit as possible and wide conductor runs employed.

Power supplies should be decoupled with tantalum or electrolytic capacitors located close to the converters. For optimum performance and noise rejection, 1μF capacitors paralleled with 0.01μF ceramic capacitors should be used as shown in the diagrams below.



POWER SUPPLY DECOUPLING

DESCRIPTION OF OPERATION—The Successive Approximation Register (SAR) is a set of flip flops (and control logic) whose outputs act as both the direct (parallel) data outputs of the Analog to Digital Converter (A/D) and the digital drive for the A/D's internal Digital to Analog Converter (D/A). See Block Diagram. Holding the A/D's START CONVERT (Pin 1) low during a clock low to high transition resets the SAR. In this state, the output of the MSB flip flop is set to logic "0", the outputs of the other bit flip flops are set to logic "1", and the STATUS output (Pin 22) is set to logic "1" (see Timing Diagram). The START CONVERT must now be brought high again for the conversion to continue. If the START is not brought high, the converter will remain in the reset state.

The D/A internal to the A/D continuously converts the A/D's digital output back to an analog signal which the comparator continuously compares to the analog input signal. The comparator output ("1" or "0") informs the SAR whether the present digital output (0111 1111 1111 in the reset state) is "greater than" or "less than" the analog input. Depending upon which is greater, on the first rising clock edge after the START has returned high, the SAR will set the MSB to its final state ("1" or "0") and bring bit 2 down to a "0". The digital output is now X011 1111 1111. The D/A converts this to an analog value, and the comparator determines whether this value is greater or less than the analog input. On the next rising clock edge, the SAR reads the comparator feedback, sets bit 2 to its final value, and brings bit 3 down to a logic "0". The digital output is now XX01 1111 1111. This successive approximation procedure continues until all the output bits are set. The rising clock edge that sets the LSB (bit 12) also drops the STATUS OUTPUT to a "0" signaling that the conversion is complete. Output data is now valid and will remain so until another conversion is started. The clock does not have to be turned off.

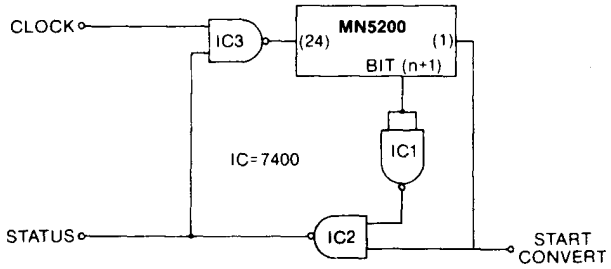
CONTINUOUS CONVERTING — The MN5200 Series A/D converters can be made to continuously convert by tying the STATUS output (Pin 22) to the START CONVERT input (Pin 1). In this configuration, STATUS (START CONVERT) will go low at the end of a conversion (see Timing Diagram) and the next rising clock edge will reset the converter bringing STATUS (START CONVERT) high again. The MSB will be set on the next rising clock edge. The result is that the STATUS will go low for approximately one clock period following each conversion. Please read the section describing the STATUS output. See below for continuous conversions while short cycling.

DIGITAL OUTPUT CODING

ANALOG INPUT				DIGITAL OUTPUT
MN5200, 5203	MN5201, 5204	MN5202, 5205	MN5206	MSB LSB
0.0000V	+5.0000V	+10.0000V	+10.0000V	0000 0000 0000
- 0.0024V	+4.9976V	+ 9.9951V	+ 9.9976V	0000 0000 0000*
- 4.9976V	+0.0024V	+ 0.0049V	+ 5.0024V	0111 1111 1110*
- 5.0000V	0.0000V	0.0000V	+ 5.0000V	0000 0000 0000*
- 5.0024V	-0.0024V	- 0.0049V	+ 4.9976V	1000 0000 0000*
- 9.9976V	-4.9976V	- 9.9951V	+ 0.0024V	1111 1111 1110*
-10.0000V	- 5.0000V	-10.0000V	0.0000V	1111 1111 1111

* Voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as 0 will change from "1" to "0" or vice versa as the input voltage passes through the level indicated. See the section on Absolute Accuracy Error for an explanation of Output Transition Voltages.
EXAMPLE: For an MN5202/05 (±10V analog input range) the transition from digital output 0000 0000 0000 to 0000 0000 0001 (or vice versa) will ideally occur at an input voltage of +9.9951 volts. Subsequently, any input voltage more positive than +9.9951 volts will give a digital output of all "0's". The transition from digital output 1000 0000 0000 to 0111 1111 1111 will ideally occur at an input of zero volts, and the 1111 1111 1111 to 1111 1111 1110 transition should occur at −9.9951 volts. An input more negative than −9.9951 volts will give all "1's".

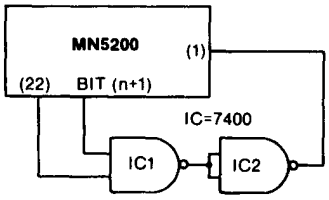
SHORT CYCLING—For applications requiring less than 12 bits resolution, the MN5200 Series A/D's can be truncated or short cycled to the desired number of bits with a proportionate decrease in conversion time. The following circuit may be used to truncate at n bits.



SHORT CYCLING SINGLE CONVERSIONS

Assuming a conversion is already in progress, bit (n+1) will go low as bit n is being set (see Timing Diagram). Since the START CONVERT signal is high at this time, STATUS (the output of IC2) will go low gating off the clock at IC3 ending the conversion. To begin a new conversion, START CONVERT is brought low driving STATUS high and gating on the clock. The first rising clock edge the converter sees with START CONVERT low will reset the converter bringing bit (n+1) high again. Now STATUS will remain high as START CONVERT is brought back high allowing the conversion to continue. Therefore, in this configuration, STATUS and START CONVERT function normally, i.e., the same as STATUS and START CONVERT for a converter not being short cycled.

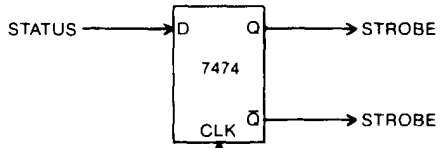
SHORT CYCLING AND CONTINUOUS CONVERTING—A previous section described how continuous converting for 12 bits could be accomplished by simply tying the STATUS output back to the START CONVERT input. To continuously convert at n bits, one simply has to tie the bit (n+1) output back to the START CONVERT input. The bit (n+1) output acts like a STATUS when one short cycles at n bits. It goes high when the converter is reset, remains a "1" during the conversion, and drops to a "0" as bit n is being set. Since it is possible for the converter to come on in any state at power-on, a lock-up condition may occur if bit (n+1) comes on as a "1" and the conversion process comes on at bit (n+2). This situation can be avoided by making the START CONVERT input the AND function of bit (n+1) and the STATUS output.

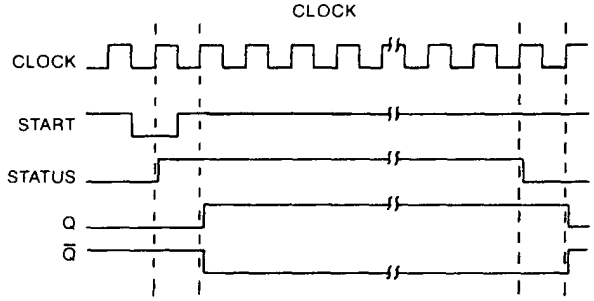


SHORT CYCLING CONTINUOUS CONVERTING

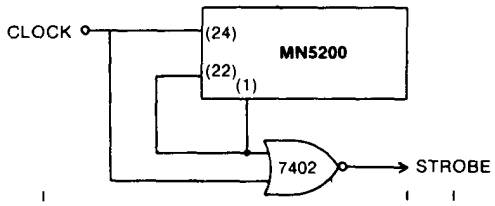
If one is already using the circuit described in the section labeled SHORT CYCLING, one can short cycle and continuously convert by making the START CONVERT input the AND function of STATUS (IC2) and STATUS (pin 7) outputs.

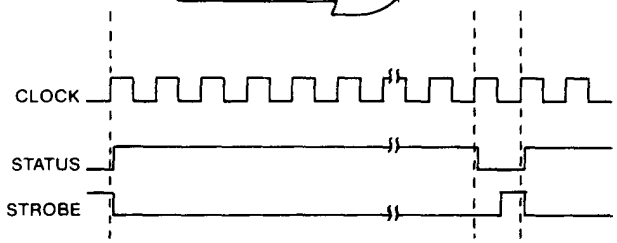
STATUS OUTPUT—The STATUS or END OF CONVERSION (E.O.C.) output will be set to a logic "1" when the converter is reset; will remain high during conversion; and will drop to a logic "0" when conversion is complete. Due to propagation delays, the least significant bit (LSB) of a given conversion may not be valid until a maximum of 30 nSec after STATUS has returned low. Therefore, an adequate delay must be provided if STATUS is to be used to strobe latches to hold output data. Simple gate delays can be employed or the STATUS can be made the input of a D flip flop whose clock input is the same as the converter clock (see sketch). In this situation, the Q output will change one clock period after STATUS changes.





If continuously converting the STATUS (E.O.C.) output can be NORed with the converter clock, as shown below, to produce a positive strobe pulse 1/2 period wide, 1/2 period after the STATUS output has gone low. The rising edge of this pulse can be used to latch data after each conversion.

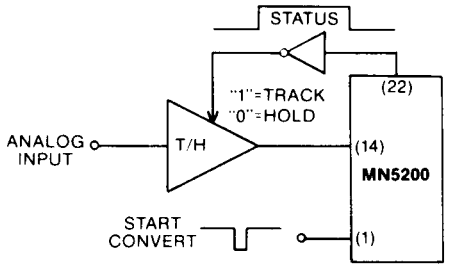




USING A TRACK AND HOLD AMP WITH MN5200 SERIES A/D's—The error that results when trying to convert moving analog signals with a successive approximation A/D can be as great as the amount the analog signal changes during a single A/D conversion time. If this error is unacceptable, a Track and Hold (T/H) or Sample and Hold (S/H) amplifier can be placed between the analog signal source and the A/D converter. A careful error analysis will be necessary to determine if the T/H is actually reducing and not increasing overall error. T/H parameters such as aperture uncertainty, gain accuracy, pedestal error and droop rate will have to be contended with (see the tutorial section of the Micro Networks'

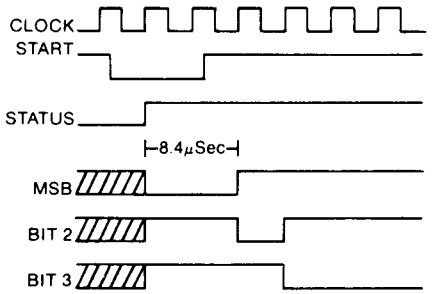
Applications Manual and Product Guide for a complete discussion of T/H parameters).

Normally, the T/H can be controlled directly by the A/D's STATUS output. Typical connections are shown below for Micro Networks' MN343 (10 μSec acquisition time to ±0.01%) and MN346 (1.6 μSec acquisiton time to ±0.01%) Track and Hold Amplifiers. The STATUS output changes form a "0" to a "1" when the converter is reset. This drives the T/H from the track to the hold mode. At the end of conversion, STATUS returns to a "0" restoring the T/H to the track mode.

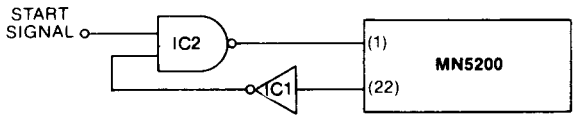


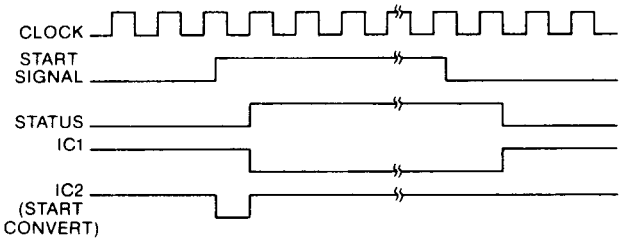
MN343		MN346
10 μSec	Acquisition Time	1.6 μSec
60 nSec	Aperature Delay	30 nSec
3 mV	Pedestal Error	2 mV
0.1 mV/mSec	Droop Rate	0.1 mV/mSec
1.5 μSec	Track to Hold Settling	150 nSec

Recall that if the START CONVERT pulse is brought high immediately after the converter has been reset, the MSB will be finalized one clock period later (see Timing Diagram). Care should be taken to ensure aperture delay time and track-to-hold settling time do not contribute errors. If necessary, the width of the START CONVERT pulse can be increased to allow more time between the T/H being commanded into the hold mode (STATUS = "1") and the MSB being set. Recall that output bits do not begin to get set until after the START CONVERT has returned high. The example below shows a 8.4 μSec delay to allow for track to hold settling. Clock frequency = 240 kHz; 1 period = 4.2 μSec.

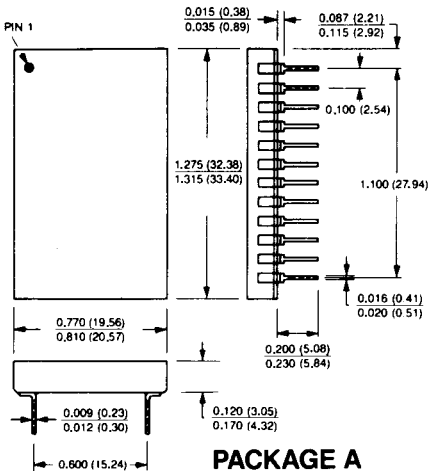


TRIGGERING WITH A POSITIVE EDGE—If it is inconvenient to generate a negative going START CONVERT PULSE of the proper width, MN5200 Series A/D's can be made to start converting on a positive going edge by employing the circuit shown below. Assuming the previous conversion is done and the Start Signal is low, the STATUS output will be low, the output of IC1 will be high, and the output of IC2 will be high. A rising edge as a Start Signal will drive the output of IC2 low. The converter will reset on the next rising clock edge. Resetting brings the STATUS high; IC1 goes low; the start Signal is still high so the output of IC2 goes high allowing the conversion to continue immediately. The Start Signal has only to be brought back down before the conversion is completed.





24 PIN DIP

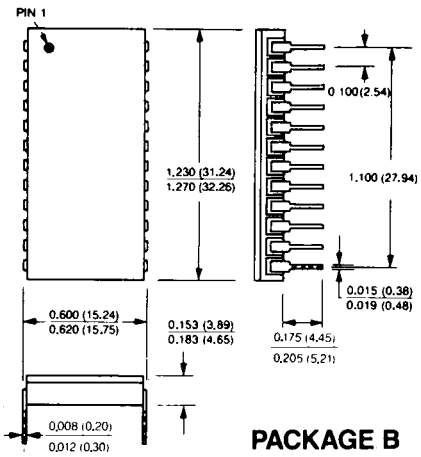


PACKAGE A

24-PIN DIP
Dimensions in Inches
(millimeters)

Note: MN5200 and MN5203 utilize package A.

MN5201, MN5202, MN5204, MN5205, and MN5206 utilize package B.



PACKAGE B