

Agile Low-Noise Frequency Synthesizer

By: A. Ridenour and R. Aurand, APITech

Abstract

Simultaneously achieving low phase noise, fast switching speed and acceptable levels of spurious outputs in microwave frequency synthesizers has long been considered difficult. Presented here is a description of a solution developed by APITech to achieve such results.

Introduction

The need for spectrally pure signal sources capable of fast frequency hopping for such applications as spread spectrum data links and Doppler radar has been growing. Traditional synthesizer architectures, such as Direct Analog Synthesis, single or multi loop analog or digital PLL's or Mix and Divide, all have weaknesses when it comes to switching time. Direct Digital Synthesis (DDS) is capable of fast switching however, from a microwave perspective, it remains in the low frequency domain.

A hybrid approach of up converting a DDS against a microwave LO signal can combine the advantages of DDS while reducing the shortcomings of other approaches.

A Hybrid Frequency Synthesizer

APITech Model 96999 is a state-of-the-art low noise frequency synthesizer targeted at applications requiring low phase noise and frequency agility. Figure 1 is a general block diagram of the frequency synthesizer.

Two architectural features are notable:

- 1) The synthesizer is built around a low noise crystal oscillator. All output frequencies from the LO Generator Module are generated by multiplying and filtering the crystal signal before mixing with a signal generated by the DDS. Clock signals for the DDS are also derived from this high performance crystal oscillator by multiplication and filtering. This technique ensures the lowest possible phase noise while retaining flexible frequency control.
- 2) The design is scalable. The native bandwidth occupies a 200 MHz slice of spectrum which may be converted anywhere within the microwave spectrum by suitable selection of multipliers and filters during the design phase. Wider bandwidths are accommodated by adding more mix/filter stages to the Upconverted Module and using appropriate RF switching networks to select the desired range.

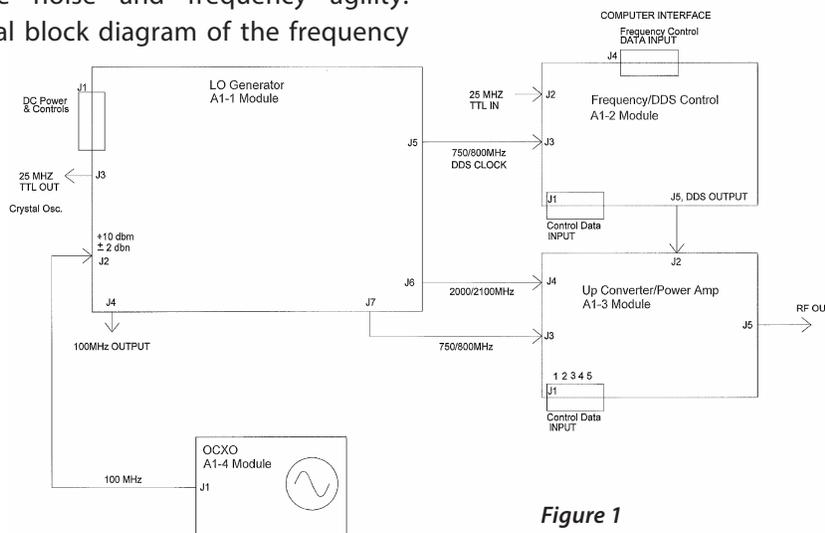


Figure 1

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Phase Noise

Figure 2 shows the single-sideband phase noise spectral density plot for a typical crystal reference oscillator employed in the model 96999 frequency synthesizer. This ovenized oscillator design is based on SC cut crystal technology.

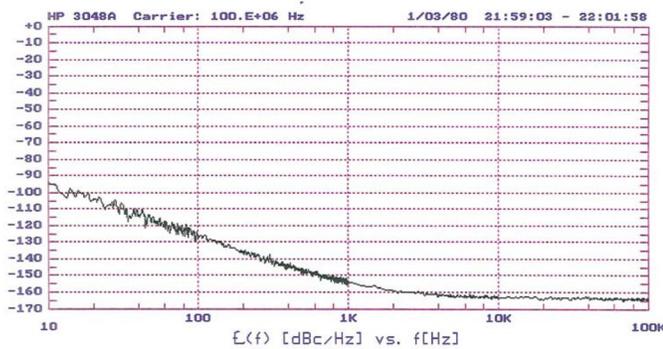


Figure 2
SSB Phase Noise of Crystal Reference Oscillator

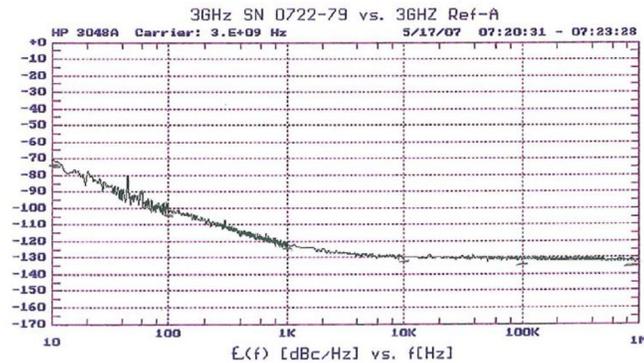


Figure 3
SSB Phase Noise of Frequency Synthesizer

Figure 3 shows the measured phase noise of a typical synthesizer when it is tuned to 3 GHz. Table 1 compares the measured phase noise densities and computes the difference between the scaled 100 MHz reference crystal oscillator and the 3 GHz output. All readings in the table are corrected by 3dB for 2 source measurement. The final column in Table 1 contains the best theoretically available phase noise, computed using the equation:

$$\text{Phase Noise} = 20 * \log(N)$$

Where

$$N = (3 \text{ GHz} / 100 \text{ MHz})$$

For the example given this equation resolves to 29.5 dB. Multiplying the 100 MHz crystal reference signal to 3 GHz will degrade the phase noise of the crystal by at least 29.5 dB.

As can be seen in the Table, at low offset frequencies the Model 96999 phase noise exceeds the 20 log(N) factor by several dB. However at 1 kHz offset the noise is approximately equal to 20 log(N). The noise situation is somewhat different at larger offset frequencies and ultimately the farther out noise floor is determined by other elements in the signal chain.

Offset Frequency	Crystal Oscillator	3 GHz output	Difference	20 log N
10 Hz	-98 dBc	-73 dBc	25 dB	29.5 dB
100 Hz	-130 dBc	-105 dBc	25 dB	
1 kHz	-155 dBc	-125 dBc	30 dB	
10 kHz	-165 dBc	-133 dBc	32 dB	
100 kHz	-167 dBc	-134 dBc	33 dB	

Table 1

The data in Table 1 describes the phase noise performance that can be achieved at any output frequency within the tuning range of the frequency synthesizer. Selection of output frequency is limited only by the step size resolution of the synthesizer. Fine step resolution is a function of the DDS programming.

Tuning Speed

Incorporating DDS technology into frequency synthesizers in this fashion brings another unique advantage to the APITech product. DDS frequency selection can be fast. Tuning speed within any 200 MHz sub-band is typically limited by the data interface, typically less than 1 µsec.

In cases where the fastest tuning speeds are desired, a wide parallel interface offers the best solution. Slower tuning speeds can be achieved with any of the I2C or serial communications protocols.

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Jumping across band segments imposes minimal switching time overhead, typically measured in 10's of nanoseconds. Band switching can be either internal, using ROM based look-up tables, or discrete band switch lines can be brought to the parallel interface for direct control.

Spurious Outputs

Whenever frequency multipliers and multiple conversions are used in a frequency generation scheme, control of spurious outputs must be taken seriously during the design and planning stages. The APITech frequency synthesizers achieve the desired low spurious levels by judicious placement of multi-pole bandpass filters in the signal path. In cases where multiple sub-bands are used, filters are switched.

Packaging

Ultimate isolation of frequency generating stages, and thus lowest possible spurious levels, demands keeping the various signal processing stages physically separated. Figure 3 shows a synthesizer configuration using multiple interconnected housings mounted on an aluminum baseplate. Also shown in the figure is an optional vibration isolation system for the crystal oscillator. More will be said about this feature later.

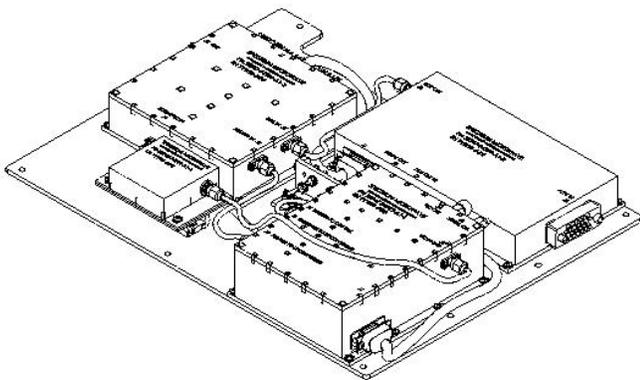


Figure 3
Mechanical Configuration

For less demanding applications a more compact arrangement can be used and this is shown in Figure 4. Also visible in this figure is a thumb-wheel switch used for selecting a nominal center output frequency. In this design variant the DDS control interface uses a serial RS-232 link allowing “steering” of the synthesizer frequency between pulses of a Magnetron Doppler Radar used for an atmospheric imaging application.

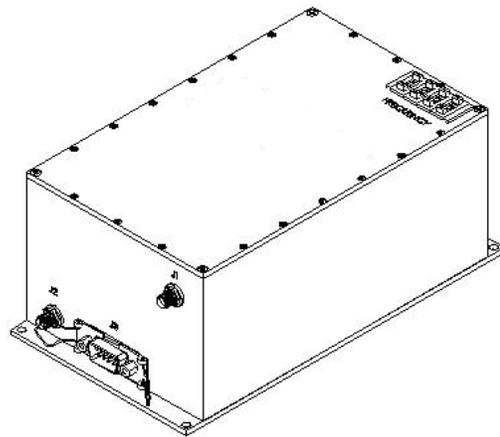


Figure 4
Compact Frequency Synthesizer

Synchronization

Some applications of low noise, fast tuning frequency synthesizers may require frequency synchronization to an external reference frequency such as Rubidium or Caesium primary standards. Or a need may exist for multiple frequency synthesizers to be operated in a master/slave configuration. To address these requirements the low-noise VHF crystal oscillator is phase-locked to the external reference signal using an additional phase locked loop.

Figure 5 shows the typical phase noise of a VHF crystal oscillator when phase locked to an external reference frequency. As can be seen, phase noise is somewhat degraded from the ideal case presented earlier using an optimized phase noise condition. Clearly seen in this graph is the noise plateau resulting from the phase detector noise floor transferring to the output of the PLL.

Many configurations using external frequency

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references are possible and optimal trade-off between loop bandwidth and phase noise is best determined at the system level.

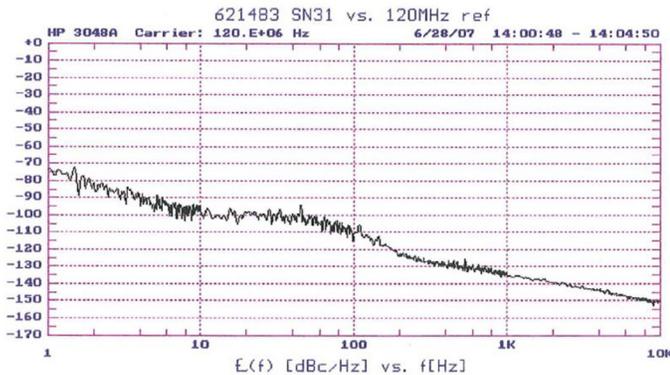


Figure 5

SSB Phase Noise of Phase-Locked Crystal Oscillator

Shock and Vibration

Many applications are subject to some physical vibration, even if it is just fan noise in equipment racks. For these situations vibration isolation of the VHF crystal oscillator is possible. A suitable strategy calls for designing the VHF oscillator mechanical assembly in a way that minimizes transmission of the vibration through the housings. Without isolation, vibration will ruin the low phase noise performance of the quartz crystals used in the VHF oscillators.

For More Information

Contact:

Art Ridenour
Sr. Technologist
APITech
1900 W. College Ave
State College, PA 16801

Conclusion

Design considerations for an agile, low noise microwave frequency synthesizer have been discussed. Some design data highlighting low phase noise has been presented. Several of the possible packaging options have been presented.

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