

High Voltage Ceramic Capacitors (HVCC)

Surface mount ceramic chip capacitor for high voltage applications

Features

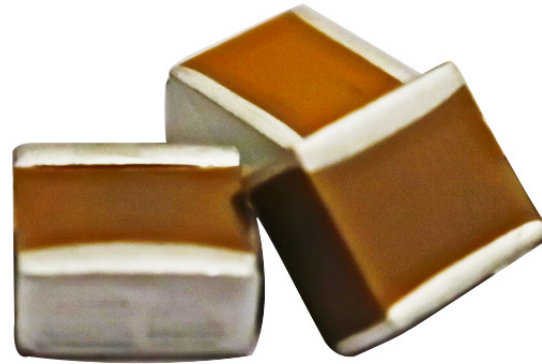
- **Voltage:** up to 2500 VDC
- **Temperature range:** -55 to 125°C
- **Termination:** fired on silver or fired on palladium silver
- **Case sizes available:** 1812, 1825, 2220, 2225, 4040, 4550

Applications

- Military power supplies
- Industrial control applications
- Medical pulse applications
- AC/DC waveform smoothing
- Filters
- Ignitors
- Power generation
- Energy storage
- Electric motors
- Pulse power/weapons
- Resonant circuits

Design and Manufacturing Overview

- Designed and produced in our State College, PA (USA) facility
- 250k sq. ft. facility with (100k sq. ft. dedicated to ceramics)
 - Variable pressure scanning electron microscope
 - Energy dispersive x-ray spectroscopy
 - Low and optical metallographic microscopes
 - Thermo graphical analysis
 - Particle size distribution and surface area analysis
- Experienced ceramics team with both design and process engineers



Advanced Ceramics Capabilities

- Research and development
- Verification
- Finishing
- Heat treatment
- Forming
- Formulating rare earth materials

HVCC Product Characteristics	
Voltage Min.	500 VDC
Voltage Max.	2500 VDC
Temperature Range	-55°C
Temperature Max. STD	125°C
Capacitance Range Min.	5000 pF
Capacitance Range Max.	0.68 μF
Termination	Silver
Termination Alt.	Palladium Silver
Size Min.	1812
Size Max.	4550
Stacked Versions	Future Development
<i>*Note: BQ, BX, BR stabilities available</i>	

High Voltage Ceramic Capacitors (HVCC)

Surface mount ceramic chip capacitor for high voltage applications

HVCC Sizes Manufactured by APITech

1812		1825		2220		2225		4040		4550	
L	.180±.012	L	.180±.012	L	.220±.012	L	.220±.015	L	.400±.020	L	.460±.020
W	.125±.008	W	.250±.015	W	.200±.012	W	.250±.015	W	.400±.020	W	.500±.025
T	.065 MAX	T	.065 MAX	T	.110 MAX	T	.110 MAX	T	.110 MAX	T	.110 MAX
MB	.24±.014	MB	.24±.014	MB	.03±.015	MB	.03±.015	MB	.03±.015	MB	.04±.020

Min. Cap.		502	502	502	502	502	502
Length	Width	500 VDC	630 VDC	1000 VDC	1500 VDC	2000 VDC	2500 VDC
18	12	333	333	183	--	--	--
18	25	503	503	333	183	822	822
22	20	503	503	333	183	822	822
22	25	224	224	104	253	103	103
40	40	504	504	334	563	223	223
45	50	684	684	474	683	333	333
Maximum Capacitance Value (EIA values available)							

Verification Process

- In-process and final testing for all customer specified parameters
- 100% Electrical testing:
 - Capacitance
 - Dissipation factor
 - Insulation resistance
 - Dielectric strength

Other Testing Available

- Internal integrity acoustic testing
- High-reliability testing via voltage conditioning and thermal shock
- Environmental testing:
 - Humidity
 - Extreme temperature
 - Barometric pressure
 - Vibration
 - Immersion
 - Solderability

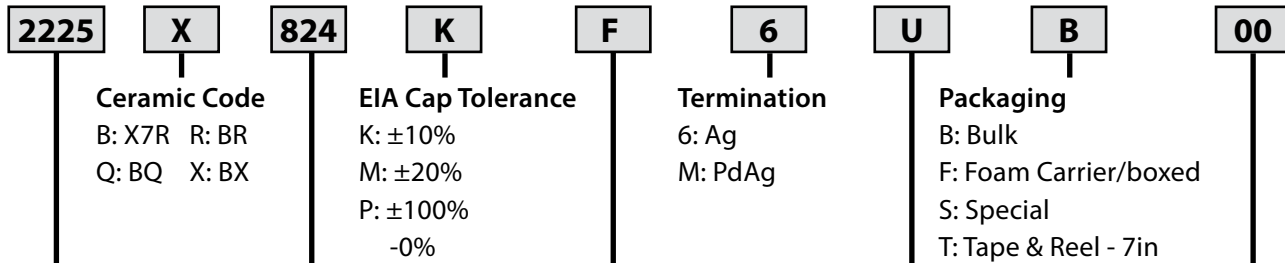
High Voltage Ceramic Capacitors (HVCC)

Surface mount ceramic chip capacitor for high voltage applications

High Voltage Ceramic Capacitors (HVCC) Part Numbering System

The part number shown represents a 2225 size high voltage capacitor. The ceramic type is X7R/BX, capacitance value is 0.82 μ F, with a tolerance of $\pm 10\%$. The voltage rating is 630 VDC, termination is "6" Ag termination, and the parts will be unmarked with bulk packaging.

Example: 2225X824KF6UB00



Case Size

Ref Dimensions Table

- A: 1812
- B: 1825
- C: 2220
- D: 2225
- E: 4040
- F: 4550

EIA Cap Code

- 824=820,000pF=0.82 μ F
- 125=1,200,000pF=1.2 μ F
- 156=15,000,000pF=15 μ F

Working Voltage

- E: 500 VDC
- F: 630 VDC
- G: 1000 VDC
- H: 1500 VDC
- J: 2000 VDC
- R: 2500 VDC

Marking

- M: Marked
- U: Unmarked

Special Requirements

- 00: Standard
- G: Custom

Soldering Guidelines

HVCCs are compatible with all soldering/mounting methods for chip capacitors.

Reflow Soldering

APITech recommends reflow soldering as the preferred method for mounting HVCCs. HVCCs can be reflow soldered using a reflow profile generally defined in IPC-FEDEC-J-STD-020. Silver termination chip capacitors are compatible with both conventional and lead-free soldering with a peak temperature of 260°C to 270°C acceptable.

The heating ramp rate should be such that components see a temperature rise of 1.5°C to 4°C

per second to maintain temperature uniformity through the HVCC.

The time for which the solder is molten, should be maintained at a minimum, so as to prevent solder leaching.

The use of an inert atmosphere can help if this problem is encountered. Palladium/Silver (Pd/Ag) terminations can be particularly susceptible to leaching with free lead, tin rich solders, and trials are recommended for this combination.

Cooling to ambient temperature should be allowed to occur naturally, particularly if larger chip sizes are being soldered.

High Voltage Ceramic Capacitors (HVCC)

Surface mount ceramic chip capacitor for high voltage applications

Natural cooling allows a gradual relaxation of thermal mismatch stresses in the solder joints. Forced cooling should be avoided as this can induce thermal breakage.

Wave Soldering

Wave soldering is not acceptable.

Solder Leaching

Leaching is the term for the dissolution of silver into the solder causing a failure of the termination system which causes increased ESR, $\tan \delta$ and open circuit faults, including ultimately the possibility of the chip becoming detached.

Leaching occurs more readily with higher temperature solders and solders with a high tin content. Pb free solders can be very prone to leaching certain termination systems. To prevent leaching, exercise care when choosing solder allows and minimize both maximum temperature and dwell time with the molten solder.

Rework of Chip Capacitors

APITech recommends hot air/gas as the preferred method of applying heat for rework. Apply even heat surrounding the component to minimize internal thermal gradients. Soldering irons or other techniques that apply direct heat to the chip or surrounding area should not be used as these can result in micro-cracks being generated.

Minimize the rework heat duration and allow components to cool naturally after soldering.

Use of Silver loaded Epoxy Adhesives

Chip capacitors can be mounted to circuit boards using silver loaded adhesive, provided the termination material of the capacitor is selected to be compatible with the adhesive. This is normally PdAg.

Handling

HVCCs should never be handled with fingers. Skin oils and perspiration and can inhibit solderability and will aggravate cleaning.

Components should never be handled with metallic instruments. Metal tweezers should never be used as these can chip the product and leave abraded metal tracks on the product surface. Plastic or plastic-coated metal types are readily available and recommended – these should be used with an absolute minimum of applied pressure.

Storage

Incorrect storage of HVCCs can lead to problems for the end-user. Rapid tarnishing of the terminations, with an associated degradation of solderability, will occur if the product comes into contact with industrial gases such as sulfur dioxide and chlorine.

Storage in moist or polluted air can result in termination oxidation.

Packaging should not be opened until the HVCCs are required for use. If opened, the pack should be re-sealed as soon as practicable. Alternatively, the contents could be kept in a sealed container with an environmental control agent.

For long term storage, conditions should, ideally, be temperature-controlled environments between -5°C and $+40^{\circ}\text{C}$ and between 40% and 60% relative humidity-controlled.

Taped products should be stored out of direct sunlight. This could promote deterioration in tape or adhesive performance.

HVCC products, stored under the conditions recommended above, in its “as received” packaging, has a minimum shelf life of 2 years.

Surface Mount Pad Design

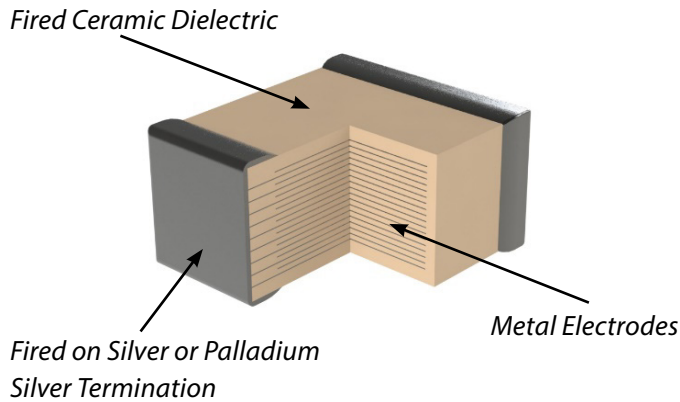
APITech's conventional 2-terminal chip capacitors can generally be mounted using pad designs in for accordance with IPC-7351, Generic Requirements Surface Mount Design and Land Pattern Standards.

High Voltage Ceramic Capacitors (HVCC)

Surface mount ceramic chip capacitor for high voltage applications

However, there are some other factors that have been shown to reduce mechanical stress, such as reducing the pad width to less than the chip width. The position of the chip on the board should also be considered.

Multilayer ceramic chip with nickel or copper barrier termination



REACH (Registration, Evaluation, Authorization, and Restriction of Chemicals) Statement

The main purpose of REACH is to improve the protection of human health and the environment from the risks arising from the use of chemicals.

RoHS Compliance

APITech routinely monitors worldwide material restrictions (EU/China and Korea RoHS mandates) and is actively involved in shaping future legislation.

Breakdown of material content, SGS analysis reports are available upon request.

Most of APITech's HVCC components are available with non-RoHS compliant tin/lead (Sn/Pb) solderable termination finish for exempt applications and where pure tin is not acceptable. Other tin-free termination finishes may also be available. Please contact us for additional details.

Ceramic Capacitors and Aging

Capacitor aging is a term used to describe the negative, logarithmic capacitance change which takes place in ceramic capacitors with time. The crystalline structure for barium titanate based ceramics changes on passing through its Curie temperature (known as the Curie Point) at about 125°C. The domain structure relaxes with time and in doing so. The dielectric constant reduces logarithmically; this is known as the aging mechanism of the dielectric constant. The more stable dielectrics have the lowest aging rates.

The aging process is reversible and repeatable. Whenever the capacitor is heated to a temperature above the Curie Point the aging process starts again from zero. The aging constant, or aging rate, is defined as the percentage loss of capacitance due to the aging process of the dielectric which occurs during a decade of time (a tenfold increase in age) and is expressed as a percent per logarithmic decade of hours. As the law of decrease of capacitance is logarithmic, this means that for a capacitor with an aging rate of 1% per decade of time, the capacitance will decrease at a rate of:

- 1% between 1 and 10 hours
- An additional 1% between the following 10 and 100 hours
- An additional 1% between the following 100 and 1000 hours
- An additional 1% between the following 1000 and 10000 hours
- The aging rate continues in this manner throughout the life of the capacitor

Typical values of the aging constant for our HVCCs are:

Dielectric Class	Typical Values
Ultra Stable C0G/NP0	Negligible capacitance loss through aging
Stable X7R	<2% per decade of time

High Voltage Ceramic Capacitors (HVCC)

Surface mount ceramic chip capacitor for high voltage applications.

Cap Size	1812					
Voltage	500	630	1000	1500	2000	2500
Cap Value (nF)						
5.0						
5.6						
6.8						
8.2						
10						
12						
15						
18						
22						
25						
27						
33						
47						
56						
68						
75						
82						
100						
120						
150						
180						
220						
270						
330						
390						
470						

Cap Size	1825					
Voltage	500	630	1000	1500	2000	2500
Cap Value (nF)						
5.0						
5.6						
6.8						
8.2						
10						
12						
15						
18						
22						
25						
27						
33						
47						
56						
68						
75						
82						
100						
120						
150						
180						
220						
270						
330						
390						
470						

High Voltage Ceramic Capacitors (HVCC)

Surface mount ceramic chip capacitor for high voltage applications.

Cap Size	2220					
Voltage	500	630	1000	1500	2000	2500
Cap Value (nF)						
5.0						
5.6						
6.8						
8.2						
10						
12						
15						
18						
22						
25						
27						
33						
47						
56						
68						
75						
82						
100						
120						
150						
180						
220						
270						
330						
390						
470						

Cap Size	2225					
Voltage	500	630	1000	1500	2000	2500
Cap Value (nF)						
5.0						
5.6						
6.8						
8.2						
10						
12						
15						
18						
22						
25						
27						
33						
47						
56						
68						
75						
82						
100						
120						
150						
180						
220						
270						
330						
390						
470						

High Voltage Ceramic Capacitors (HVCC)

Surface mount ceramic chip capacitor for high voltage applications.

Cap Size	4040					
Voltage	500	630	1000	1500	2000	2500
Cap Value (nF)	500	630	1000	1500	2000	2500
5.0						
5.6						
6.8						
8.2						
10						
12						
15						
18						
22						
25						
27						
33						
47						
56						
68						
75						
82						
100						
120						
150						
180						
220						
270						
330						
390						

Cap Size	4550					
Voltage	500	630	1000	1500	2000	2500
Cap Value (nF)	500	630	1000	1500	2000	2500
5.0						
5.6						
6.8						
8.2						
10						
12						
15						
18						
22						
25						
27						
33						
47						
56						
68						
75						
82						
100						
120						
150						
180						
220						
270						
330						
390						

Processing & Soldering Notes

General Soldering Recommendations for Leadless Ceramic Capacitors

Soldering Ceramic Capacitors with High Temperature Process

SN10 Solder

Ramp Rate, Heating and Cooling: Approx. 30°C/min.

Peak Temperature: Approx. 320°C

Dwell at Peak: <30 Seconds

Soldering Ceramic Capacitors with Medium Temperature Process

SN96 Solder

Ramp Rate, Heating and Cooling: Approx. 30°C/min.

Peak Temperature: Approx. 250°C

Dwell at Peak: <30 Seconds

Soldering Ceramic Capacitors with Low Temperature wProcess

SN62 Solder

Ramp Rate, Heating and Cooling: Approx. 30°C/min.

Peak Temperature: Approx. 220°C

Dwell at Peak: <30 Seconds

Notes

Care must be taken to minimize the time silver terminations are exposed to molten solder to avoid leaching (amalgamation of the silver into molten solder). APITech recommends the use of a silver (Ag) bearing solder when terminating directly to ceramic ceramic capacitors to reduce the potential for leaching. Gradual heating and cooling of the components are essential to prevent thermal stresses to the ceramic.

Application Note: Soldering Recommendations for Switch Mode Power Supply Capacitors

- SMPS capacitors are highly durable structures designed to provide long service per lifetime, however they require attention to basic considerations during assembly. Like all ceramic components, SMPS capacitors are subject to thermal stresses. For this reason, preheating of the capacitor assemblies is recommended. Preheat components using hot plate to 120 to 150°C, or within 50 to 60°C of the soldering temperature being applied. Avoid over-exposure to high temperatures during assembly and allow for gradual, post-assembly cooling.
- For hand iron soldering, recommended soldering iron tip temperature is 330 to 350°C. Contact the pad adjacent to the pre-tinned lead should be made from below the PCB (opposite of the component side), and the dwell time on the solder joint should be less than five seconds. An aluminum heat sink plate may be placed adjacent to the SMPS lead frame to protect the ceramic body during assembly. Avoid direct contact between soldering iron and ceramic during assembly process. Soldering time is dependant upon heat sinking provided by the chassis and boardmaterial, so a longer preheat cycle may be required.
- Standard solders (Sn60, Sn63, Sn60/38/2) may be used. Please consult the factory for use with RoHS compliant solders.
- Use a controlled temperature profile ramp not exceeding 4°C per second as measured by an attached low mass thermocouple.
- Soldering time and temperatures can vary with component size, board material and layout. Please consult the factory for assistance.